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Trap density probing on top-gate MoS_2 nanosheet field-effect transistors by photo-excited charge collection spectroscopy†

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Two-dimensional (2D) molybdenum disulfide (MoS_2) field-effect transistors (FETs) have been extensively studied, but most of the FETs with gate insulators have displayed negative threshold voltage values, which indicates the presence of interfacial traps both shallow and deep in energy level. Despite such interface trap issues, reports on trap densities in MoS_2 are quite limited. Here, we probed top-gate MoS_2 FETs with two- (2L), three- (3L), and four-layer (4L) MoS_2/dielectric interfaces to quantify deep-level interface trap densities by photo-excited charge collection spectroscopy (PECCS), and reported the result that deep-level trap densities over 10^{12} cm^{-2} may exist in the interface and bulk MoS_2 near the interface. Transfer curve hysteresis and PECCS measurements show that shallow traps and deep traps are not that different in density order from each other. We conclude that our PECCS analysis distinguishably provides valuable information on deep level interface/bulk trap densities in 2D-based FETs.

After graphene, two-dimensional (2D) dichalcogenide semiconductors appeared as new candidates for 2D nanoelectronics, and molybdenum disulfide (MoS_2) nanosheets are some of them.[1–3] MoS_2 shows a distinct intrinsic band gap depending on the sheet thickness[4–8] although its mobility is less than that of graphene, a gapless semiconductor.[9–12] MoS_2 nanosheet field-effect transistors (FETs) have thus been extensively studied with bottom- or top-gate structures, while the top-gate one using high-k dielectrics is regarded as being more suitable for practical applications with patterned gates.[8,13–20] Still, MoS_2 channel formation is mostly implemented by mechanical exfoliation using scotch tape and most FETs with gate insulators have displayed negative threshold voltage values,[8,13–16,21–23] which indicates the presence of interfacial traps both shallow and deep in energy level. Moreover, the threshold voltages are not reproducibly acquired even by fixed insulator deposition and exfoliation conditions. Despite such interface trap issues, reports on trap densities in MoS_2 are quite limited.[21,22,24–27] In the present study, we probed top-gate FETs with two- (2L), three- (3L), and four-layer (4L) MoS_2/top-dielectric interfaces to quantify deep-level interface/bulk trap densities particularly by photo-excited charge-collection spectroscopy (PECCS),[28–30] and reported the result that deep-level trap densities over 10^{12} cm^{-2} may exist at the top high-k dielectric/MoS_2 interface and the MoS_2 layer as well.

A surface-cleaned 285 nm-thick SiO_2/p^+-Si wafer was chosen as the substrate for our MoS_2 nanosheet top-gate transistor. The MoS_2 flakes were exfoliated mechanically from bulk MoS_2 crystals and transferred to the substrate by using a scotch tape technique. The samples were dipped in acetone for 30 min to remove any residue and dried with N_2 gas after methyl alcohol rinsing. The layer number of the exfoliated MoS_2 flakes was confirmed by Raman spectroscopy. For the source (S) and drain (D) electrodes, Au/Ti (50/25 nm) were deposited and patterned on the flakes using photo-lithography, lift-off, and DC-sputter deposition processes. As the first process layer, the lift-off layer (LOL: LOL 2000, Micro Chemical) was coated and thermally cured at 438 K for 5 min. Then, the photo-resist layer (PR: SPR 3612, Micro Chemical) as the second process layer was coated and baked at 388 K for 2 min. The samples were exposed to UV light for 5 s through our S/D patterned photomask by using a photo-aligner. The samples were patterned with a metal-ion-free (MIF) developer solution. A 25 nm-thin Ti and 50 nm-thin Au layer were deposited sequentially by a DC magnetron sputtering system. For the lift-off process to finely define the S/D electrode, acetone and LOL remover solvents were used. Thermal annealing was carried out at 473 K for 10 min in a N_2 atmosphere to improve contact resistance, removing any PR residue (see ESI 1†). A 50 nm-thin Al_2O_3 gate dielectric layer was deposited at 373 K using atomic layer

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deposition (ALD) and finally 50 nm-thin indium-tin-oxide (ITO) was deposited on Al_2O_3 for a transparent gate electrode. To pattern the gate electrode, the same processes were implemented as were performed for the S/D electrodes. All electrical measurements of our transistors were performed with a semiconductor parameter analyser (Model HP4155C, Agilent Technologies) in the dark and with ambient air at room temperature. The PECCS measurements were carried out with the same electrical measurement setup but under an optical probe that uses a 500 W Hg(Xe) arc lamp as a light source, a grating monochromator, and an optical fiber (core diameter of 200 μm). The average optical power density of the monochromatic light was ~0.1 mW cm^{-2} as measured after the light passed through the optical fiber.

Fig. 1a, b, and c show optical microscope (OM) images of 2L, 3L, and 4L MoS_2-based top-gate transistors on 285 nm-thick SiO_2/p^+-Si. Each inset photograph shows the magnified images of the Au/Ti S/D electrodes and the MoS_2 flakes before the ITO top-gate electrode is deposited. The ITO top-gate electrode is transparent enough to show the MoS_2 channel underneath. Under the OM the MoS_2 image contrast strongly depends on the layer number and we thus exploit this feature to select flakes with a large enough area and uniform thickness. However, the images of 2L, 3L, and 4L are barely distinguishable as respectively identified in Fig. 1a, b, and c, since the three are quite similar in thickness. Our MoS_2 nanosheet flakes were ~10 μm on one side, so that a 6 μm-long channel was available for our device. The average width (W)/length (L) ratios of 2L, 3L, and 4L are 2.68, 0.67, and 1.46, respectively. The layer number was more precisely identified using the Raman spectra in Fig. 1d.[31] The vibrational peaks at 382.7, 381.6, and 381.2 cm^{-1} correspond to the in plane (E^1_{2g}) modes of the 2L, 3L, and 4L layer MoS_2 while those at 403.7, 404.8, and 405.7 cm^{-1} are attributed to the out of plane (A_{1g}) modes of the 2L, 3L, and 4L layer MoS_2. The vibration frequency differences between these two modes are 21.0, 23.2, and 24.5 cm^{-1} for the 2L, 3L, and 4L MoS_2 flakes respectively. The inset in Fig. 1d shows the atomic displacement schemes of the Raman-active modes, E^1_{2g} and A_{1g}. Fig. 1e illustrates the three-dimensional schematic view of the transparent top-gate transistor with the MoS_2 nanosheet, the Al_2O_3 dielectric layer and the ITO top-gate electrode under monochromatic light for the PECCS measurements.

Fig. 2a, b, and c display the drain current–gate voltage (I_D–V_G) transfer characteristics of the 2L, 3L, and 4L MoS_2 nanosheet transistors, respectively. According to the drain current–drain voltage (I_D–V_D) output characteristics at various V_G values shown in Fig. 2d, e and f, the Au/Ti S/D contacts are quite ohmic for all FETs, although some contact resistance would be expected from the FET with the 2L nanosheet. The on/off current ratio of all transistors is ~10^6 with a high on-current of a few μA (the gate leakage current, I_G, is also shown to be a few pA). The linear mobilities (μ_{lin}) are respectively estimated to be 3.1, 1.4, and 2.1 $cm^2\ V^{-1}\ s^{-1}$ as the maximum values for the 2L, 3L, and 4L MoS_2 transistors, when they are plotted as a function of V_G (shown in the respective insets).

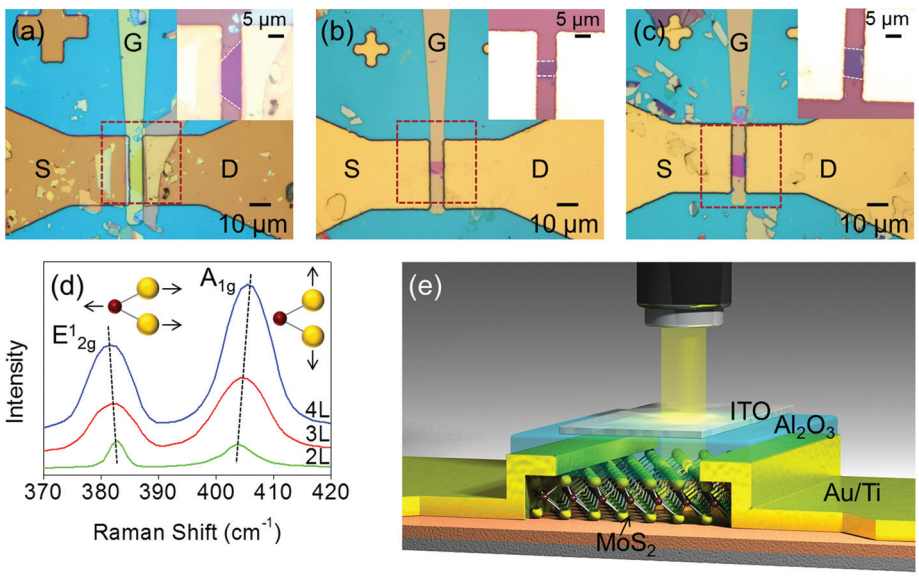

Fig. 1 Optical microscopy (OM) images of the (a) two-layer (2L), (b) three-layer (3L), and (c) four-layer (4L) MoS_2-based top-gate transistor on top of a silicon substrate with 285 nm-thick SiO_2. Each inset photograph shows a magnified image of the Au/Ti source/drain electrodes and the exfoliated MoS_2 before patterning of the ITO top-gate electrode. (d) Raman spectra of the 2L, 3L, and 4L MoS_2 flakes with the inset showing the atomic displacement of the two representative Raman-active modes: E^1_{2g} and A_{1g}. (e) Three-dimensional schematic view of a top-gate transistor with a single-layered MoS_2 nanosheet, an Al_2O_3 dielectric layer and ITO as a top-gate electrode under monochromatic light for the photo-excited charge-collection spectroscopy (PECCS) measurements. (The transmittance of the light was more than 80% after passing through the Al_2O_3 and ITO, ESI 2†).

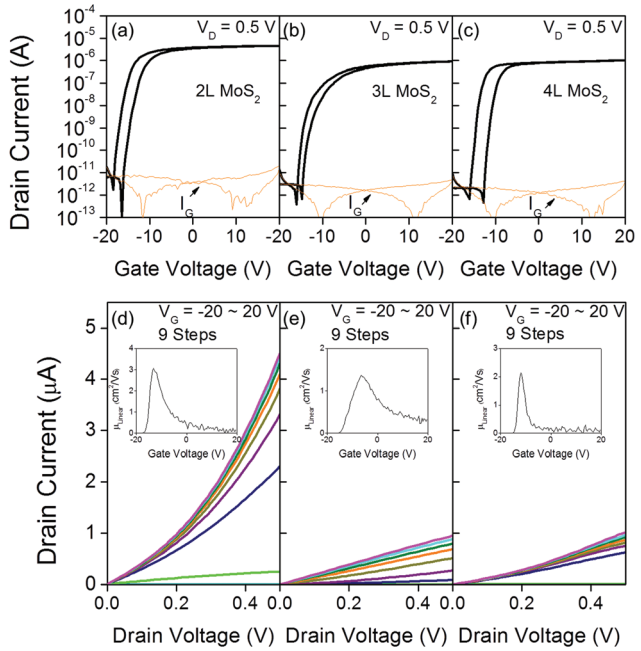

Fig. 2 Drain current–gate voltage (I_D–V_G) transfer curves of the top-gate transistors with (a) 2L, (b) 3L, and (c) 4L MoS_2 as obtained at V_D = 0.5 V. I_G indicates the gate leakage current. Drain current–drain voltage (I_D–V_D) output curves of the (d) 2L, (e) 3L, and (f) 4L MoS_2-based transistors with a V_G sweep from −20 V to +20 V (9 steps). The respective inset curve shows the V_G-dependent linear mobility plots.

The mobility was estimated using the following well-known equation:[13,15]

$$\mu_{lin} = \frac{\partial I_D}{\partial V_G}\frac{1}{C_{ox}V_D(W/L)} \quad (1)$$

where C_{ox} is the dielectric capacitance per unit area.

All the transistors show a large negative threshold voltage (V_{Th}) of −12∼−18 V. In classical reasoning, this might be due to the positive fixed charges introduced during the ALD process in the Al_2O_3 dielectric layer or at the MoS_2 channel/Al_2O_3 dielectric interface.[22,24] The positive charge generates a negative shift in the flat-band voltage (V_{FB}) (that would contribute to the same amount of V_{Th} shift) where V_{FB} is described below:[32]

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{x_{ox}} \frac{x}{x_{ox}}\rho(x)\mathrm{d}x \quad (2)$$

where Φ_{MS} is the metal–semiconductor work-function difference, Q_f is the fixed trap charge per unit area near the channel/dielectric interface, $\rho(x)$ is the charge density of the bulk traps in the gate dielectric, and x_{ox} is the dielectric thickness. However, if the ALD process also introduced such charges into the MoS_2 channel as dopants and impurities making the channel more conductive, the flat band voltage equation, eqn (2), should be modified and the threshold voltage equation should also be modified, to result in much more negative values. In fact, we have several evidences for the ALD-induced doping effects in ESI 3.† In all the ALD dielectrics, such doping effects are quite apparent. Although such threshold voltage modifications might be too complex to be considered here, we could properly modify eqn (2) for the V_{FB} by newly defining Q_f as below, since our channels are only a few nm thin:

$$Q_f = Q_{it} + Q_{bt} = Q_{it} + qN_{bt}t \quad (3)$$

where Q_{it} is the trap charge per unit area at the interface and Q_{bt} is for the near-interface bulk trap charges which can be described as $qN_{bt}t$, while q is an electronic charge, N_{bt} is the volume density of the bulk traps near the interface and t is the MoS_2 thickness.

The transfer curves show a hysteresis, which was here defined as the variation of V_{Th} (ΔV_{Th}) at I_D = 1 nA when V_G is swept from −20 V to 20 V (forward) and then swept back (reverse) to −20 V. The hysteresis values for 2L, 3L, and 4L are estimated to be 2.45, 1.60, and 3.15 V, respectively. This is probably due to the shallow level positive charges located at the MoS_2/Al_2O_3 interface which can trap/detrap electrons during the forward/reverse V_G sweep. The amount of trap charge density is approximately estimated to be 1.92×10^{12}, 1.26×10^{12}, and 2.47×10^{12} q cm^{-2} for the 2L, 3L, and 4L MoS_2 transistors using the following equation and also assuming that the trap charge density at the dielectric/semiconductor interface is only influential and those in the dielectric oxide are mostly not:

$$\Delta Q = \Delta V_{Th} C_{ox} \quad (4)$$

This estimation does not give any energy level information of the deep traps, stemming only from the charges shallow enough to be trapped/detrapped under the gate bias sweep. According to the hysteresis direction (clockwise), the trapped charges are regarded as electrons. There are a few papers regarding hysteresis in top-gated MoS_2 transistors, but still the nature of this has not been fully understood.[21,33,34]

As a more general approach for the near-interface trap analysis, the subthreshold swing (SS) was measured from the same transfer curves: the SS values were 0.39, 0.44, and 0.50 V dec^{-1} for the 2L, 3L, and 4L MoS_2 transistors, respectively, when obtained using $(\mathrm{d}\log(I_D)/\mathrm{d}V_G)^{-1}$ in an I_D range from 10 to 100 pA. The SS of the transistor is related to the interface trap density (D_{it}) *i.e.* the average density of state (DOS) for the dielectric/semiconductor interface traps, and the bulk trap density (N_{bt}) *i.e.* the DOS for the bulk of the semiconductor near the interface, based on the following equation:[23]

$$SS = ln(10)\left(\frac{kT}{q}\right)\left[1 + \frac{q}{C_{ox}}\left(\sqrt{\frac{\varepsilon_{ch}N_{bt}}{kT}} + qD_{it}\right)\right] \quad (5)$$

where kT = 0.026 eV at room temperature and ε_{ch} is the dielectric constant of a 2D or thin-film semiconductor. Using the SS values and by setting N_{bt} = 0, the maximum D_{it} values are estimated to be 4.33×10^{12}, 5.00×10^{12}, and 5.78×10^{12} cm^{-2} eV^{-1} for the 2L, 3L, and 4L MoS_2 transistors respectively, and it should be noted that this average D_{it} may include the densities

from both the shallow and deep level traps (both at the interface and the semiconductor bulk near the interface). The difference between the D_{it} values among 2L, 3L, and 4L is marginal but still worth considering. This difference could be understandable because in the common sense the thicker nanoflakes (4L) might have more interlayers (as trapping sites) than the thinner (2L or 3L) ones. The higher trap density estimated by SS than by hysteresis is also understandable, since the SS-driven value reflects both the shallow and deep traps in density while the hysteresis reflects only the shallow ones.

Our top-gate MoS_2 transistors were also subjected to positive bias stress (PBS) under the conditions V_G = 20 V and V_D = 0.5 V while the stress was stopped at approximately logarithmic time intervals to measure the transfer curves of our transistors. Fig. 3a, b, and c show the final states of the transfer characteristics of the 2L, 3L, and 4L MoS_2 transistors after 3600 s, respectively as overlaid on their initial states. According to the figures, the curves gradually moved to the positive side but by only a small amount of ΔV_{Th} without much SS or hysteresis change. The shift was so minimal that the PBS-driven trap charge density with electrons might be estimated to be less than 5×10^{11} q cm^{-2} from the $\Delta V_{Th} C_{ox}$ calculation in eqn (4). These results may indicate that both the 2D channel surface and the dielectric oxide in our top-gate MoS_2 transistors are surprisingly strong and resistant against electrical stress, although they surely have ALD-induced charges inside. Charges inside the dielectric turned out not to be influential to the hysteresis under gate stress and sweep as we assumed in previous paragraphs for Fig. 2. [Such bias stress resistance was hardly shown in the single-crystalline ZnO nanowire-based FETs with ALD Al_2O_3 dielectric, indicating that the MoS_2 surface is much more flawless than that of the ZnO nanowire. (ESI 4†)]

We have discussed so far the shallow trap charge density estimated by hysteresis and the average density of state, D_{it}, which is summed and averaged over the whole sub band gap range. Here we also probed the deep trap charges near the interface with a quantification method, PECCS measurements,

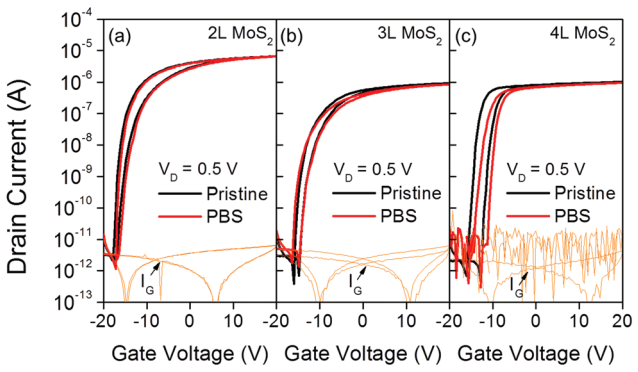

Fig. 3 Transfer curves of the (a) 2L, (b) 3L, and (c) 4L MoS_2-based transistors after 3600 s period positive gate bias stress (PBS) under V_G = 20 V and V_D = 0.5 V, as overlaid on their respective initial transfer curves.

for the 2L, 3L, and 4L MoS_2 transistors.[28–30] As a first step, photo-induced transfer curves were measured sequentially by applying monochromatic photons in the wavelength range from 1800 nm (0.69 eV) to 600 nm (2.07 eV) with an interval of 5 nm. The V_G sweep started from the channel accumulation to the depletion state because we should initially fill up all the interface trap states with charge carriers prior to every photo-excitation. When photons with a certain energy (ε) illuminate the region near the channel/dielectric interface, most of the trap charges (electrons) trapped in the gap states between the conduction band minimum (CBM) and the CBM-ε are excited to the CBM level. Hence the initial fixed charge Q_f near the interface is varied to $Q_{eff}(\varepsilon)$, which is mainly for the traps remaining at and near the channel/dielectric interface. The light-induced effective trap charge modulation ($\Delta Q_{eff}(\varepsilon)$) is acquired by the shift of V_{FB} ($\Delta V_{FB}(\varepsilon)$) which is the difference between the photo-induced V_{FB} and the initial V_{FB}. The relationship can be expressed as follows:[28–30]

$$\Delta V_{FB}(\varepsilon) = -\frac{\Delta Q_{eff}(\varepsilon)}{C_{ox}}$$

where

$$\Delta Q_{eff}(\varepsilon) = Q_f - Q_{eff}(\varepsilon) \quad (6)$$

$$Q_{eff}(\varepsilon) = q \int_{VBM}^{CBM-\varepsilon} D_{it}(\varepsilon) d\varepsilon \quad (7)$$

where CBM and VBM are the conduction band minimum and the valence band maximum, respectively. Then, D_{it} has a relationship with V_{FB}:

$$D_{it}(CBM - \varepsilon) = -\frac{C_{ox}}{q} \frac{\partial V_{FB}(\varepsilon)}{\partial \varepsilon} \quad (8)$$

Fig. 4a, b, and c show the transfer curves of the 2L, 3L, and 4L MoS_2 transistors under several monochromatic photons along with the dark transfer curve. Based on the series of photo-induced transfer characteristics of the transistors at a fixed V_D = 0.5 V, we estimated the photo-induced negative $\Delta V_{FB}(\varepsilon)$ and calculated $\Delta Q_{eff}(\varepsilon)$ with respect to the photon energy (ε), using eqn (6). Fig. 4d shows the $|\Delta Q_{eff}(\varepsilon)|$ plot as a function of ε for the 2L, 3L, and 4L MoS_2 transistors. The deep trap charge density monotonously increases without showing any rapid increase in intensity until the photon energy reaches the band edge (starting at 0.69 eV). Moreover, such monotonous increase was more obvious with the thicker MoS_2. These results suggest two strong probabilities in our measurement: (1) most of the deep traps broadly exist above a level of CBM = 0.69 eV, located near the top-gate interface (which means both the interface and the 2–4L thin bulk). There have been some reports about theoretical predictions of deep states like a sulfur vacancy with an energy level 0.4–0.6 eV below the CBM,[35–37] which our light source for the PECCS measurements cannot provide due to its own lowest photon energy limit at 0.69 eV. The detailed nature of such dopant and trap impurities near the interface is not identified yet, and will be discussed in a future study along with the ALD-induced doping. (2)

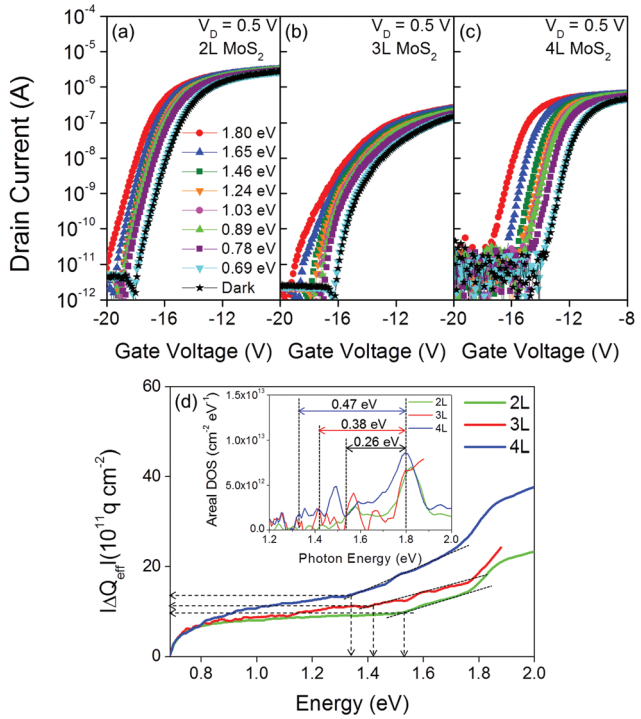

Fig. 4 Photo-induced transfer curves of the (a) 2L, (b) 3L, and (c) 4L MoS_2-based transistors under monochromatic light of various wavelengths for the PECCS measurements. (d) Photon energy-dependent effective trap charge modulation (ΔQ_{eff}) plots for the 2L, 3L, and 4L MoS_2-based transistors. The black dotted lines with arrows indicate the indirect band gap transition regions and the total ΔQ_{eff} values within the sub band gap region for the 2L, 3L, and 4L MoS_2 whereas the inset shows the density of states (D_{it}) profile that may indicate the onset of the first indirect gap (1.54, 1.42, and 1.33 eV respectively for 2L, 3L, and 4L) and the second direct gap energy (1.80 eV).

Our eqn (3) is consistent with our PECCS data, where $|\Delta Q_{eff}(\varepsilon)|$ increases monotonously with the thickness, because Q_{it} should be the same regardless of thickness but Q_{bt} ($= qN_{bt}t$) should increase with the thickness or layer number.

On the one hand, a somewhat rapid increase of $|\Delta Q_{eff}(\varepsilon)|$ appears to start near 1.54 eV for 2L, 1.42 eV for 3L, and 1.33 eV for 4L as indicated by the arrows, whose values are consistent with the previously reported indirect band-to-band transition of MoS_2 nanosheets.[7,8] Therefore, according to the plots, the density values for the sub band gap trap charge (Q_f or maximum ΔQ_{eff}) are now estimated to be ~1.00×10^{12}, 1.15×10^{12}, and 1.37×10^{12} q cm^{-2} for the 2L, 3L, and 4L transistors, respectively. [So, we could actually separate the average Q_{it} and N_{bt} values as 0.7×10^{12} q cm^{-2} and 2.8×10^{18} cm^{-3}, respectively, based on the t-dependent $|\Delta Q_{eff}(\varepsilon)|$ plots from the 2L, 3L, and 4L MoS_2 transistors (see ESI 5† for more details).] These deep trap charge densities are not higher than the shallow trap charge densities estimated by hysteresis. The sums of the deep and shallow trap densities appear to be ~2.92×10^{12}, ~2.41×10^{12}, and ~3.84×10^{12} cm^{-2} for the 2L, 3L, and 4L transistors, respectively. These sums are smaller than those estimated by SS, since the SS-driven average

Table 1 Summary of the hysteresis, PECCS, and SS estimated trap densities

Number of MoS_2 layers	Trap density ($\times 10^{12}$ cm^{-2}) obtained from: Hysteresis	PECCS	Hysteresis & PECCS	SS
2	1.92	1.00	2.92	6.67
3	1.26	1.15	2.41	7.10
4	2.47	1.37	3.84	7.69

D_{it} × energy gaps (1.54, 1.42, and 1.33 eV for 2L, 3L, and 4L MoS_2) work out to be 6.67×10^{12}, 7.10×10^{12} and 7.69×10^{12} cm^{-2} for the 2L, 3L, and 4L transistors, respectively. This difference in the sum may be attributed to the limit of the SS equation (eqn (5)) which reflects any influence by contact resistance. However, the values from SS and hysteresis/PECCS are of the same order of magnitude and are comparable to each other. The trap density values estimated from the SS, hysteresis, and PECCS measurements are summarized in Table 1 for a more detailed comparison.

As a by-product, the PECCS-driven D_{it} plot is shown in the inset of Fig. 4d, where a D_{it} peak intensity of about 4.0×10^{12} cm^{-2} eV^{-1} is displayed near the band edges (onset region: 1.54, 1.42, and 1.33 eV) for the 2L, 3L, and 4L transistors, while the direct band-to-band transition of MoS_2 *i.e.* the second band gap is also observed with a large threshold shift in the photo-induced transfer curves at 1.80 eV for both transistors as shown in Fig. 4a, b, and c. We thus regard our PECCS measurements as providing quite valuable information in both respects: the near-interface trap density of the MoS_2 FETs and the indirect/direct optical gap of the 2D MoS_2.

As a final brief concern, we have considered extracting out the contact resistance-exempted linear mobilities of the 2L, 3L, and 4L MoS_2 FETs from their respective transfer and output curves in Fig. 2 (see ESI 6† for the detailed extraction methods[38]), since their field mobility values appear to be quite smaller than the generally reported ones; such small mobilities would be mainly due to coulomb and surface roughness scatterings by ALD-induced impurities and pin-holes,[39–41] but partially because of large contact resistances. As a result, 19.4, 1.44, and 1.7 cm^2 V^{-1} s^{-1} were respectively achieved as contact resistance-free mobilities from the 2L, 3L, and 4L MoS_2 FETs, which had field mobilities of 3.1, 1.4, and 2.1 cm^2 V^{-1} s^{-1}. The 7 times-enhanced mobility of the 2L MoS_2 indicates that it has a higher Schottky barrier and contact resistance due to its larger band gap than those of the thicker MoS_2 channels.

Conclusions

In summary, we have fabricated top-gate 2D MoS_2 FETs for 2L-, 3L-, and 4L-thin channels with ITO gate electrodes, to probe the shallow and deep level traps located at or near the dielectric ALD-grown Al_2O_3/MoS_2 interface. Transfer curve hysteresis

and PECCS measurements show that the shallow traps and the deep traps are not much different in density order from each other. The total trap density estimated by SS, and PECCS and hysteresis displayed about the same order as a few number $\times 10^{12}$ cm^{-2} for both cases, however the SS-driven trap density always appears relatively higher because it can not exclude the influence of contact resistance. The PECCS analysis directly distinguishes the near-interface deep traps unlike other methods,[21,22,24–27] even separating the interface trap charge (Q_{it}) and the near-interface bulk traps (Q_{bt}/or N_{bt}). We thus conclude that our PECCS analysis provides valuable information on the deep level near-interface trap density of top-gate few layer MoS_2 FETs.

Acknowledgements

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