Few-Layer MoS₂–Organic Thin-Film Hybrid Complementary Inverter Pixel Fabricated on a Glass Substrate

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Molybdenum disulfide (MoS₂), a dichalcogenide compound has recently been studied as one of new important 2D semiconductors beyond graphene,¹–⁶ the well-known gapless 2D semiconductor, since MoS₂ has a discrete energy band gap over ~1.2 eV.⁷–¹² Mechanical exfoliation and direct imprint-to-transfer of MoS₂ nanosheets/orakes have mostly been implemented for device fabrications,¹³,¹⁴ while large scale direct growth is recently in progress.¹⁵–²⁰ Mobilities of the MoS₂ nanosheets in field effect transistor (FET) range from 0.1 to a few hundreds cm² V⁻¹ s⁻¹ for exfoliated or imprinted MoS₂ sheets⁴–⁶ and those obtained from direct growth show only a few cm² V⁻¹ s⁻¹ or below yet.¹⁵–²⁰ In respects of functional applications, photodetectors,²¹–²⁴ gas sensors,²⁵,²⁶ and logic inverters²⁷–²⁹ have been reported to see any prospects of MoS₂ nanosheet-based electronics. As another reachable applications, display pixel backbone, and peripheral logic devices on glass or plastic substrate were suggested with optical microscope (OM) images for bottom gate MoS₂ FET image, another OM image showing several nano-flakes but without device pattern is found. Among the nanoflakes, the thinnest one in the center is tri-layer (3L) MoS₂ that we utilized for the FET. Comparing the two images of blue boxes for FET and nanoflakes only, we may notice that the central 3L-thin flake was actually captured by source/drain electrodes for channel; it is not observed as laid below opaque metal electrodes, but three other flakes (indicated by 1, 2, and 3) surrounding the central one clearly prove that the 3L-thin flake is the channel. A schematic 3D image of the device is shown in Figure 1c, where Au is commonly used for top-gate of n-channel 3L-thin MoS₂ FET and for bottom-gate of p-channel heptazole FET as well [the surface morphology of heptazole thin film is seen in the inset atomic layer between mechanically exfoliated MoS₂ channel and oxide dielectric, we could successfully match the both transfer curves of p-channel organic and n-channel 2D layer FETs, to practically realize the hybrid-CMOS inverter. Such modified mobility was ~6 cm² V⁻¹ s⁻¹, which is still much higher than the value of recently reported large area MoS₂ nanosheets.¹⁸,²⁰ Our hybrid-CMOS inverter shows a voltage gain of more than 12 and a few hundred pW power consumption at a low operation voltage, also demonstrating a high switching frequency over 480 Hz with a few tens of μs delay due to minimum parasitic capacitance, one of the benefits from glass substrate. Our 2D nanosheet-organic semiconductor hybrid inverter basically utilizes a vertical device architecture on glass, however, it appears planar because the channel dimension (a few μm) of MoS₂ is incomparably smaller than that of organic channel (~100 μm). Despite the huge differences in dimension (width, length, and thickness), our inverter nicely operates as a light detecting pixel as well, since it contains MoS₂ channel FET on glass. This type of hybrid approach is unprecedented but not so much difficult and rather realistic, enabling 2D nanoelectronics to extend their application toward display and pixel electronics.

Figure 1a displays a snap shot photo and a photographic image of our hybrid-CMOS inverter device on glass, along with optical microscope (OM) images for bottom gate organic FET (red box ~2.2× magnified from photographic image) and top-gate 2D MoS₂ FET (blue box ~40x). At a glance, it is clearly noted that the MoS₂ channel dimension is much smaller than that of organic channel. Below the MoS₂ FET image, another OM image showing several nanoflakes but without device pattern is found. Among the nanoflakes, the thinnest one in the center is tri-layer (3L) MoS₂ that we utilized for the FET. Comparing the two images of blue boxes for FET and nanoflakes only, we may notice that the central 3L-thin flake was actually captured by source/drain electrodes for channel; it is not observed as laid below opaque metal electrodes, but three other flakes (indicated by 1, 2, and 3) surrounding the central one clearly prove that the 3L-thin flake is the channel. A schematic 3D image of the device is shown in Figure 1c, where Au is commonly used for top-gate of n-channel 3L-thin MoS₂ FET and for bottom-gate of p-channel heptazole FET as well [the surface morphology of heptazole thin film is seen in the inset atomic

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force microscopy (AFM) image, while the molecular structure of heptazole (C_{26}H_{16}N_{2}) is also shown in p-channel FET illustration of Figure 1c. More details for device fabrication and dimensions (including W/L ratio) are explained in the Experimental Section, Table 1, Table S1, and Figure S1, Supporting Information. Figure 1b is Raman spectroscopy data proving the thickness of our MoS_{2} to be 3L (as indicated by frequency peak separation between E_{2g}^1 and A_{1g} vibration ≈23 cm^{-1}).[34–36]

As seen in the 3D scheme of Figure 1c, we insert a 30 nm-thin buffer layer CYTOP between atomic layer deposited (ALD) Al_{2}O_{3} (70 nm) and MoS_{2} channel to reduce the dielectric capacitance, and so as to modify the threshold voltage of n-channel FET. (It is quite understandable because more positive gate voltage is necessary for FET channel with low capacitance dielectric to accumulate the same density of electron carriers as that by high dielectric capacitance.) According to the drain current–gate voltage (I_D–V_G) transfer curves of MoS_{2} FETs in Figure 2a,b, their threshold voltages are obviously too much shifted toward negative side if FETs are only with thin Al_{2}O_{3} (50 nm). It is also observed from the curves of 3L, 10L, and 20 nm-thick (=30L) MoS_{2} FETs that thinner MoS_{2} channel results in smaller threshold voltage along with lower I_D, whether the FETs have CYTOP buffer or not. The threshold voltages of 3L- and 10L-thin MoS_{2} FETs with 50 nm-thin ALD Al_{2}O_{3} were around −15 and −25 V, respectively (Figure 2a), however those were reduced to less than −4 and −6 V by increasing the Al_{2}O_{3} thickness to 70 nm and inserting 30 nm-thin CYTOP buffer between Al_{2}O_{3} and MoS_{2} channel as observed in Figure 2b. Figure 2c,d respectively displays drain current–drain voltage (I_D–V_D) output curves obtained from 3L MoS_{2} FETs without and with buffer layer. According to the output curves, our MoS_{2} nanosheet has good ohmic contact with source/drain (S/D) electrodes in both cases. The insets of Figure 2c,d show the capacitance–voltage plots of gate dielectrics as measured from respective

Table 1. Electrical properties of 3L and 10L MoS_{2} FETs with and without CYTOP layer.

<table>
<thead>
<tr>
<th></th>
<th>V_th [V]</th>
<th>W/L</th>
<th>I_on [A]</th>
<th>ON/OFF ratio</th>
<th>SS [V dec^{-1}]</th>
<th>μ_{p linear} [cm^{2} V^{-1} s]</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/o CYTOP 3L MoS_{2}</td>
<td>−12.85</td>
<td>1.11</td>
<td>1.57 × 10^{-5}</td>
<td>4.2 × 10^{4}</td>
<td>1.03</td>
<td>6.2</td>
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<tr>
<td>W/o CYTOP 10L MoS_{2}</td>
<td>−25.5</td>
<td>0.95</td>
<td>3.25 × 10^{-6}</td>
<td>1.1 × 10^{8}</td>
<td>0.66</td>
<td>12.7</td>
</tr>
<tr>
<td>With CYTOP 3L MoS_{2}</td>
<td>−3.2</td>
<td>1.14</td>
<td>2.09 × 10^{-7}</td>
<td>3.2 × 10^{4}</td>
<td>0.45</td>
<td>6.0</td>
</tr>
<tr>
<td>With CYTOP 10L MoS_{2}</td>
<td>−5.7</td>
<td>1.00</td>
<td>2.83 × 10^{-6}</td>
<td>6.5 × 10^{7}</td>
<td>0.55</td>
<td>14.9</td>
</tr>
</tbody>
</table>

Figure 1. a) Snap shot and photographic view of a hybrid-CMOS inverter device fabricated on glass with zoomed images for bottom-gate organic FET (2.2×, red box) and top-gate 2D MoS_{2} FET (40×, blue box). Another blue box image shows the initials flakes before device patterning proving that the central nanoflake is the channel we used for 3L-MoS_{2} FET. b) Raman spectra for 3L-MoS_{2} nanosheet. (The local vibration peak difference between E_{2g}^1 and A_{1g} is 23 cm^{-1}.) c) Schematic 3D view of our hybrid-CMOS inverter where Au is commonly used for top-gate of n-channel 3L MoS_{2} FET and for bottom-gate of p-channel heptazole FET as well (inset: AFM image of organic heptazole film surface.)
FETs, and the measured capacitances were 152 nF cm\(^{-2}\) for 50 nm ALD Al\(_2\)O\(_3\) and 35.5 nF cm\(^{-2}\) for 70 nm Al\(_2\)O\(_3\)/30 nm CYTOP. We also summarize the maximum linear mobility, subthreshold swing (SS), threshold voltage (\(V_{th}\)), ON/OFF \(I_D\) ratio, \(I_{D,ON}\) current of our 2D FETs in Table 1. The linear mobility of 3L MoS\(_2\) FET was estimated to be \(\approx 6\) cm\(^2\) V\(^{-1}\) s\(^{-1}\) whether it has CYTOP buffer dielectric or not, while those of 10L-thick MoS\(_2\) FETs were 12–15 cm\(^2\) V\(^{-1}\) s.

**Figure 3** shows a front view cross section of our hybrid-CMOS inverter, which thus appears as a vertical structure with top organic p-channel heptazole FET (with bottom gate) and bottom 3L-thin MoS\(_2\) FET (with top gate). This front cross section view is expected from the 3D device scheme in Figure 1c. According to the cross section view, top heptazole layer is supported by thin organic CYTOP over 100 nm-thick Al\(_2\)O\(_3\), which is probably useful for good interface matching between organic channel and oxide dielectric (here, we achieved a comparably decent heptazole FET mobility of \(\approx 0.14\) cm\(^2\) V\(^{-1}\) s\(^{-1}\)).**

Dynamic inverter switching has also been measured from our hybrid-CMOS inverter and its behavior is displayed in Figure 3e,f when the device is switched by \(V_{in}\) under a \(V_{DD}\) of 2 V. ON (\(V_{in} = -4\) V, \(V_{out} = 2\) V) and OFF (\(V_{in} = 2\) V, \(V_{out} = 0\) V) states are then acquired at two different frequencies: 10 Hz (Figure 3e) and 480 Hz (Figure 3f). resistor-capacitor (RC) switching delay might not be clearly measured due to the limit of equipment capacity, however, is assured to be less than few tens of ms (according to Figure 3f).

Since our hybrid-CMOS inverter contains MoS\(_2\) channel which has energy band gap less than 1.8 eV and is also attached to the glass substrate\([40–43]\), it could operate as a light-detecting pixel whose general and schematic layout is found in Figure S2, Supporting Information. Photograph in
Figure 4a displays the pixel operation by our hybrid-CMOS device, which is now illuminated by green light through the glass from the bottom. (Inset illustrates the pixel operation with a front cross section view of the CMOS pixel.) Under the illumination of red and green light emitting diodes (LEDs, 1.4 mW), initial VTC curve moves toward more negative side as shown in Figure 4b. These curve shifts were mainly observed from bottom illumination through the glass substrate (see inset circuit of Figure 4c), while top illumination (inset circuit of Figure 4f) to the inverter appeared not much effective for the VTC shift as seen in Figure 4e. It is because 70 nm-thick Au common gate electrode blocks the light penetration to MoS₂ channel, while the organic heptazole is almost transparent with its band gap higher than 2.9 eV (green light has only 2.3 eV).[33] These differences between bottom and top illumination were again observed by the photo-induced |DD of the hybrid-CMOS pixel. According to the photo-induced |DD curves in Figure 4c,f, bottom-illumination causes much higher photo-current in the pixel than top-illumination (the small amount of photo-current under top-illumination may be attributed to the interface/or surface charge traps in the organic FET). Dynamic pixel operations are observed by ON/OFF switching of bottom LED light when recorded at fixed V in voltages of −3.1 V (for red) and −3.7 V (for green detection) as shown in Figure 4d. Such V in was properly determined to obtain a maximum photo-induced V out from red and green, based on the photo-induced VTC curves in Figure 4b. The pixel dynamics was quite fast with photo-response of less than 100 ms, and real time photo-response is provided in a short video file (hybrid-CMOS pixel.avi in the Supporting Information).

As a final experimentation, we fabricated a few more hybrid-CMOS inverters on glass substrate controlling the CYTOP thickness for heptazole FET, to confirm and modify the hybrid-CMOS device performances. Figure S3, Supporting Information shows the results from one of the devices. According to Figure S3a, Supporting Information, the threshold voltage of organic heptazole FETs has changed toward more positive from that of our previous organic FET in Figure 3c, and so does the transition voltage of VTC.

Figure 3. a) Front-side cross sectional view of our hybrid-CMOS inverter device with n-channel MoS₂ and p-channel heptazole. It looks vertical in front-side view. b) |D–|V D output curves of p- and n-channel FETs that present somewhat symmetrical behavior each other. The inset shows a circuit of the vertical hybrid-CMOS inverter. c) Respective |D–|V G transfer curves of n-channel MoS₂ and p-channel heptazole FETs as obtained at V G of 1 and −1 V. d) The voltage transfer characteristics (VTCs) of our hybrid-CMOS inverter device under supply voltages (V DD) of 1≈5 V along with the inset plots for voltage gains. The dashed curve shows power consumption at 1 V operation. Peak was quite less than 1 nW. VTC output/inverting dynamics obtained at e) 10 and f) 480 Hz frequencies under square wave input pulses.
Voltage gain was ≈10 under 5 V $V_{DD}$ (Figure S3c, Supporting Information) and the peak power consumption at 1 V operation was only 1 nW (Figure S3d, Supporting Information). Since the transition voltage changed from $-4$ to 1 V, this newly fabricated hybrid-CMOS may be more ideal toward an enhanced mode device. Similar photo-response to the previous figure (Figure 4c) was observed from the newly fabricated device in Figure S3e, Supporting Information. Therefore, our hybrid-CMOS inverter comprised of organic and 2D channel FETs on glass is regarded quite promising in logic and pixel application as well.

In summary, we have fabricated a hybrid-CMOS logic inverter comprised of top-gate n-channel MoS$_2$ nanosheet FET and bottom-gate p-channel organic heptazole FET on a glass substrate. Our 2D nanosheet-organic semiconductor hybrid inverter utilizes a vertical device architecture where top-gate MoS$_2$ FET and bottom gate organic FET use a common gate electrode. Controlling the threshold voltage and drain current of MoS$_2$ FET with MoS$_2$ thickness and organic CYTOP buffer layer, we could successfully match the both transfer curves of p-channel organic and n-channel 2D layer FETs, and finally achieved a practical hybrid-CMOS inverter. Our hybrid-CMOS inverter shows a voltage gain of more than 12 and only a few hundred pW power consumption peak, also demonstrating a display-compatible switching frequency over 480 Hz with a few tens of µs delay. It was also found that our hybrid-CMOS inverter well operates even as a pixel by itself containing visible light-detecting MoS$_2$ channel on glass, although MoS$_2$ dimension was incomparably smaller than that of organic heptazole layer. We conclude that our 2D nanosheet-organic semiconductor hybrid approach for CMOS inverter is novel and promising enough to merge 2D nanoelectronics and future display/pixel applications.

**Experimental Section**

*Device Fabrication:* MoS$_2$ nanoflakes were mechanically exfoliated from bulk MoS$_2$ crystals (SPI supplies, natural molybdenite) and transferred to cleaned glass substrate (Corning, Eagle 2000) by using a standard scotch tape method. For the n-channel S and D ohmic contact electrodes, Ti/Au (25/50 nm) were patterned (deposited at room temperature) on top of MoS$_2$ nanoflakes (for instance, see the dashed line-indicated 3L flake found from glass substrate in Figure S1, Supporting Information) by using photolithography, lift-off, and DC-sputter deposition processes. (The n-channel FET has a channel length (L) of 4 µm and width (W) of ≈4 µm.) As the first layer, the spin coating process was performed to form the lift-off layer (LOR 3A, Micro Chemical) and photo-resist (AZ GXR-601, AZ electronic materials) layers. Then the samples were exposed to UV light for 5 s under photo-mask aligner for S/D pattern. After developing patterns, Ti/Au bilayer was deposited by DC magnetron sputtering system. The lift-off process was
done using acetone and LOR remover. After that, the device was annealed at 250 °C with N₂ flow in rapid thermal annealing (RTA) system for 10 min, to remove polymer residue and simultaneously to reduce contact resistance. As a gate insulator, a 30 nm thick CYTOP was spin-coated and thermally cured at 180 °C for 120 min, followed by a 70 nm thick Al₂O₃ was deposited on the MoS₂ nano flakes using atomic layer deposition system (ALD) at 100 °C. As a common gate of MoS₂ and heptazole transistors, Au (70 nm) electrode was patterned by lift-off process. Then 100 nm thick Al₂O₃ was deposited again as a gate insulator of heptazole transistor. For an organic interface matching, a 30 nm thin CYTOP was spin-coated on the 100 nm-thick ALD oxide and thermally cured at 180 °C for 120 min. Then, 50 nm thick organic crystalline heptazole was thermally deposited through a shadow mask as an active channel layer by organic molecular beam deposition system at a deposition rate of 0.1 nm s⁻¹ and at room temperature. (Crystallinity of monolayer heptazole layer is also shown as CuKα X-ray diffraction spectra in Figure S4, Supporting Information.) Finally, a 100 nm thick Au was thermally evaporated and patterned as a source/drain and interconnection. (The p-channel FET has a L of ≈21 plus Program.

Supporting Information is available from the Wiley Online Library.

Supporting Information

Table S1, Supporting Information, shows the properties of our hybrid CMOS. The width-to-length (W/L) ratios of our FETs are ≈600 µm, and thickness details of our vertical type CMOS inverter structure are again shown in the Supporting Information. The authors acknowledge the financial support from NRF (NRL program: Grant No. 2014R1A2A1A0100448), Nano-Materials Technology Development Program (Grant No. 2012M3A7B4034985), and Brain Korea 21 plus Program.


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